Sirus T2
Application Note

Anisotropic Dielectric Removal vs. Sequential Removal

Depending on the desired information, delayering of the integrated circuit is usually performed by either of two strategies: (a) anisotropic removal of all dielectric layers, or (b) sequential removal of all layers including conductors.

Anisotropic removal of dielectric layers (“Skeleton Etch”)

In this procedure, all dielectric layers are removed anisotropically down to the silicon surface. Metal conductors will be left sitting on top of pedestals of dielectric material, see figure 1. An anisotropic etch must be used to prevent undercut of the metal lines, or else the stress in the metal will usually cause delamination. When the silicon dioxide etch approaches the polysilicon gate material, a CF_4 + CHF_3 gas mix is used to improve selectivity to silicon and decrease erosion of the polysilicon lines.

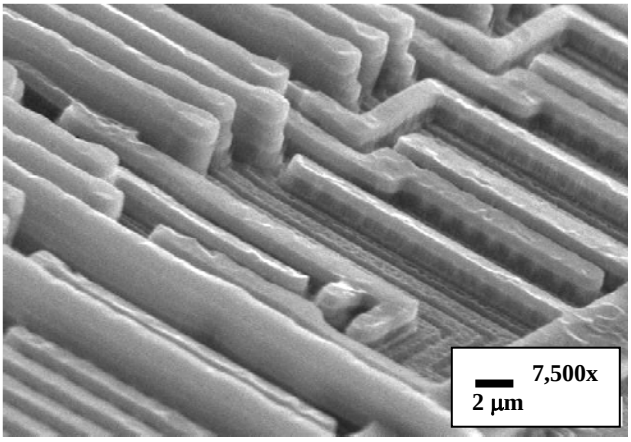

Fig. 1. “Skeleton” etch sequential removal.

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Sequential Removal

Anisotropic dielectric removal is useful, but in many situations defects or other features of interest may lie underneath conductors. In this case, metal and dielectric layers must be removed sequentially. Naively, one would expect that a simple reversal of the etch processes used to fabricate the circuit would delayer it. However, it is important to remember that when reactive ion etching is performed during fabrication there is photoresist on the circuit surface to cover up areas that should not be etched, and each etch step usually terminates on an “etch stop”, i.e. a layer which has a very low etch rate for the etch. During sequential delayering, neither of these things is true.

Proper etch recipe selection is crucial to prevent inadvertent removal of layers not intended to be etched. It is important that lower level metals layers are not exposed when the top level metal is etched, or the lower level metals will be removed prematurely.

Planar Delayering

In order to maintain planarity during sequential delayering of an IC, it is desirable to stop each dielectric etch when a level is reached that is even with the next metal layer to be etched. Thus when the passivation is etched, it should be etched level with the base of the metal line. Since there is no etch stop between the dielectric layers, this process requires a timed etch. The time will have to be determined by trial and error for any given integrated circuit process using several test pieces for process development. Failure to time the etch process properly will result in a metal line that is either sitting on top of an oxide pedestal, or contained within a trough. Once the metal line is removed, this pedestal or trough geometry will be propagated downward during the next oxide etch step because the oxide etch is anisotropic. If delayering is not done in a planar fashion, more and more topography will be created that will propagate downward, leaving a very irregular surface. If the objective is simply to remove all metal and dielectric layers so defects on the polysilicon can be viewed, it is probably easiest to dip the part in dilute HF (hydrofluoric acid). HF will isotropically etch all dielectric materials and will undercut the metal lines, thus removing all conductors except the polysilicon.

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