Plasma Delayering of Integrated Circuits

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Introduction

Increased circuit densities, smaller feature sizes and ever increasing multilayer technologies have created many challenges for today’s failure analysis engineer. Wet etch techniques have long been unable to do an acceptable job deprocessing and even many dry etch techniques fall short in etching the more difficult ICs. This paper gives a brief introduction to the basic concepts in plasma processing, discusses today’s state-of-the-art techniques for dry processing in failure analysis and provides an outline of dry etch recipes for etching critical layers on new technologies. Also discussed are solutions to the major pitfalls of dry etching such as RIE grass and keeping devices active.

Plasma Basics

What is a plasma?

Plasma is called, by many, the fourth state of matter. It is different from the other three, in that it contains free disassociated electrons and ions in a balanced steady-state condition. This, by definition, is a plasma. A plasma contains in a disassociated state: free radicals, ions, electrons and unexcited molecules. The ratio of the ions to the rest of the molecules constitutes the “ion density” of the plasma. The plasma has a net charge of zero, hence equal numbers of positive and negative charges.

For practical use, a plasma is simply a method for turning nonreactive molecules into electrically charged reactive molecules. Many safe inert gases when broken up yield extremely reactive by-products. Freons, for instance, are extremely long lived inert compounds but when broken up they yield relatively large concentrations of fluorine and chlorine (some of the most reactive compounds known). Since this process is controlled directly from the application of an electric field, the reactivity and directionality of the process can be controlled by the applied power. This flexibility and control is what makes plasma processing useful.

How are plasmas made?

Plasma is made by introducing energy into matter. This is accomplished in many ways, such as: through heat, radiation and (as in our case) an electric field. The ionization rate determines the plasma’s electron energy. Regular plasmas exhibit ionization rates of 0.001%, but high-density plasmas or HDP have an ionization rate of approximately 1%. The following is a simple illustration of ionization where a neutral molecule or atom collides with an electron to produce an ion and another electron.

\[ e^- + A \rightarrow A^+ + 2e^- \]

When a molecule or atom is exited to a higher energy state by the collision of an electron it stays in that energy state for a short period and then returns to its natural relaxed state. When that happens, energy is emitted in the form of a photon. Since different atoms or molecules emit light at different wavelength, different gases display distinctive plasma glow colors. This makes the use of spectrometers for end point detection a very useful one as wavelength peaks are used to determine when a certain layer has been removed.

\[ e^- + A \rightarrow A^* + e^- \]

\[ A^* \rightarrow A + h\nu \text{ (photon)} \]

The plasmas used in semiconductor processing are very specific in nature. Processing semiconductor devices requires a relatively low temperature plasma. To create this low temperature plasma, the plasma has to be created through the application of an electric field to conductive gases. Fortunately, gases are electrically conductive at easily achieved, moderately low pressures (on the order of 1 Torr).

History of Plasma Reactors

Plasma processing was introduced to the Semiconductor Industry in the 60s. The first systems were of the “Barrel” type and were typically used for stripping photoresist. Previous to this time, wet chemical solvents were used. These solvents were potentially carcinogenic and expensive to dispose of. Plasma processing, on the other hand, is far more effective in removing positive resist, uses orders of magnitude less chemicals, and is therefore far more kind to the environment.
**Barrel Reactors**

The first barrel systems were inductively coupled (see figure 1) and consist of a quartz bell jar with a coil wrapped around it, turned on its side. Since the quartz chambers etch in fluorinated gas, these systems are usually only used to strip photoresist with oxygen. Later versions of barrel systems were capacitively coupled and consist of a cylindrical aluminum chamber with an inner concentric cathode (figure 2). Since the anode in capacitively coupled barrels is the barrel wall itself, these barrels can be made of aluminum; and because the aluminum is inert to the fluorinated etch gas, these systems can be used for etching.

**Parallel Plate Reactors**

Parallel Plate reactors (see figure 3) are by definition capacitively coupled, they are either bottom or top powered. Etching in a top powered reactor is referred to as “Plasma mode” etching or “PE mode” and etching a bottom powered reactor it is referred to as “Reactive Ion Etching”. This is a bit of a misnomer, because both systems are generically “plasma etchers”.

**Fig. 1. Inductively Coupled Barrel.**

**Fig. 2 Capacitively Coupled Barrel.**

Despite the fact this is an older technology and they etch isotropically (due to the chamber geometry), barrel systems are very versatile and are still widely used in the industry today.

**Parallel Plate Reactors**

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**Fig. 3. Parallel Plate Reactor.**

The first widely used Parallel Plate Reactor was the “Reinburg” reactor (see figure 4), which was developed at Texas Instruments in 1972. There are many variants of this design, but they are all basically a bottom powered electrode system, large enough to accommodate twenty five, 100 mm wafers.

**Fig. 4. Reinburg Reactor.**

The first fully automated, single wafer parallel plate system was introduced to semiconductor production lines in 1979, by Tegal corporation. Because of the superior process results that single wafer systems offer, almost all production etch systems are of this configuration.

**Reactive Ion Etching**

The name “Reactive Ion Etching” is misleading. It really should be called “Ion Assisted Etching”. The percentage of ions in a plasma is very small, and if they were the only species participating, the overall etch rate would also be very small. The actual mechanism is a three step process:

1. Chemical adsorption of reactive molecules (free radicals) on the surface.
2. Impact of an ion on the surface (reactive or not).
3. Physical disassociation of many reaction by-products from the surface.

Reactive Ion Etch processes (see figure 5) were, until the late 80’s, the only production plasma processes that produced an anisotropic etch. This phenomenon is a result of the chamber geometry, plasma physics and operating pressures of the systems. In general, two things define Reactive Ion Etching, a bottom powered reactor and an operating pressure below 100-
mTorr. This is also misleading, because these are only two contributing factors in achieving an anisotropic etch.

Fig. 5. Reactive Ion Etch Configuration.

Hybrid Reactors (Triode, ECR and ICP)
Within the last few years, there have been many new types of reactors introduced into the industry. These are Triode, ECR (or downstream microwave) and ICP reactors. We call these “Hybrid” reactors, because they introduce power into the reactor through a secondary source. This is advantageous, because you can add power to the plasma without coupling it through the sample. These types of reactors or secondary power sources excite the plasma to produce high density plasma (HDP). Hybrid reactors, therefore, have much lower charge damage, sputtering and operating temperature; and they have higher etch rate and selectivity.

Plasma Etch Chemistries
The five most common materials that are etched in deprocessing ICs are: polyimide, silicon nitride, silicon dioxide, aluminum and polysilicon. Table I shows the most common etch chemistries for each of these materials. Later in the article, a more detailed discussion of these chemistries and why each are used for each material is provided.

<table>
<thead>
<tr>
<th>Material</th>
<th>Etch Gases</th>
<th>Reactive Species</th>
<th>By-product</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polyimide</td>
<td>1st step: O₂ / 6% CF₄ 2nd step: 50% O₂ / Ar</td>
<td>Monatomic oxygen and/or ozone with the C from CF₄ aiding in organic removal</td>
<td>CO and H₂O</td>
</tr>
<tr>
<td>Silicon Nitride</td>
<td>Freon 14 (CF₄) or SF₆ / 10% O₂</td>
<td>Free fluorine</td>
<td>SiF₄ and N₂</td>
</tr>
<tr>
<td>Silicon Dioxide</td>
<td>CF₄ / 10% O₂</td>
<td>CF⁺⁺⁺, CF⁺⁻</td>
<td>SiF₄ and CO</td>
</tr>
<tr>
<td>Aluminum</td>
<td>Boron Trichloride (BCl₃) and Chlorine (Cl₂)</td>
<td>Free chlorine</td>
<td>AlCl₃</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>CF₄ / SF₆ 10% O₂, or Chlorine</td>
<td>Free fluorine or free chlorine</td>
<td>SiF₄ or SiCl₄</td>
</tr>
</tbody>
</table>

Table I. Common materials and etch chemistries.

Basic Deprocessing Recipes

Polyimide
There are many varieties of polyimide on the market today. They have different curing properties, solids content, etc. However, they are all hydrocarbons, and most etch readily in oxygen plasmas. This reaction is a simple oxidation of the organics as shown in the following equation:

\[
\text{CxHy (s) + O}_2 (g) + \text{plasma} \rightarrow \text{CO (g) + H}_2\text{O (g)}
\]

The main problem, in the removal of polyimide, is insuring that the polyimide does not over heat during the process. If this occurs the polyimide can carbonize, leave a grass like residue, and be virtually impossible to get off. Reducing the ion bombardment solves this problem; running very low power, and/or “floating” the sample in the plasma, and/or using a hybrid reactor can accomplish this.

A good starting recipe for polyimide* removal is given in Table II.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td>200-mTorr</td>
<td>Relatively high pressure = low voltage</td>
</tr>
<tr>
<td>Power (RIE/ICP)</td>
<td>20 / 500-watts</td>
<td>Relatively low power low voltage</td>
</tr>
<tr>
<td>O₂ / CF₄</td>
<td>47 / 3-sccm</td>
<td>Sufficient flow for most processes</td>
</tr>
<tr>
<td>Etch Rate</td>
<td>1-μm/min</td>
<td></td>
</tr>
</tbody>
</table>

Table II. Polyimide etch recipe.

*Note: Running a 50% O₂/Ar step after the polyimide has been almost completely removed, <50-nm remaining, can drastically improve the cleanliness of the results. The conditions are just like the ones listed in Table II, with the obvious change from O₂/CF₄ to O₂/Ar. Since polyimide is usually followed by a layer that does not etch in oxygen or argon (nitride/oxide), over-etching is not an issue.

Silicon Nitride
Silicon nitride typically comprises the final passivation layer of an IC. It etches readily in plasmas that contain a lot of free fluorine (such as SF₆/O₂ or CF₄/O₂ plasmas). The SF₆ is isotropic by nature. However, in this case, this property is actually advantageous in removing the nitride sidewalls surrounding top metal.

The equation for this reaction is:

\[
\text{Si₃N₄ (s) + SF₆ + plasma} \rightarrow \text{SiF₄ (g) + SF₂ (g) + N₂ (g)}
\]

A good starting recipe for nitride is:
### Table III. Nitride etch recipe.

**Silicon Dioxide**

There are many types of silicon dioxide in use today. They all etch in the same chemistry, however the recipes and etch rates vary a little with the type. Typically, highly doped oxides etch faster and oxides with high carbon content etch dirtier. The chemical reaction for this process is given below:

\[
\text{SiO}_2 (s) + \text{CF}_4 (g) + \text{plasma} \rightarrow \text{SiF}_4 (g) + \text{CO} (g)
\]

Silicon dioxide etching is intrinsically anisotropic due to the fact that the strong chemical bond between the silicon and oxygen requires ion bombardment to break.

A good starting recipe for top layer SiO$_2$ is:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td>150-mTorr</td>
<td>Relatively high pressure = low voltage</td>
</tr>
<tr>
<td>RIE Power</td>
<td>100-watts</td>
<td>Relatively low power = low voltage</td>
</tr>
<tr>
<td>SF$_6$ / O$_2$</td>
<td>45 / 5-sccm</td>
<td>Sufficient flow so SF$_6$ is not a rate limiting factor, with 10% oxygen helping accelerate the etch rate.</td>
</tr>
<tr>
<td>Etch Rate</td>
<td>0.2-um/min</td>
<td></td>
</tr>
</tbody>
</table>

### Table IV-a. SiO$_2$ etch recipe.

If an ILD (inter-layer dielectric) etch is desired where the ILD is SiO$_2$ a different process is recommended. The process relies on very low pressures to avoid grass formation. Running the process at lower pressures increases the Mean Free Path (MFP) and thus the IC’s surface is bombarded with more reactive species that possess more energy. Low RIE power or voltage is used to maintain the IC’s functionality and allow less heat build up on it. ICP power is used to maintain a relatively high etch rate by creating a HDP. This process is listed in Table IV-b:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td>5-mTorr</td>
<td>Very low pressure to reduce grass formation</td>
</tr>
<tr>
<td>Power (RIE / ICP)</td>
<td>30 / 350-watts</td>
<td>Relatively low RIE power = low voltage</td>
</tr>
<tr>
<td>CF$_4$ flow</td>
<td>25-sccm</td>
<td>Lower flow for less polymerization, and no oxygen so erosion or metal lifting does not affect the aluminum lines.</td>
</tr>
<tr>
<td>Etch Rate</td>
<td>0.1-um/min</td>
<td></td>
</tr>
</tbody>
</table>

### Table IV-b. ILD etch recipe.

**Aluminum**

Pure aluminum, by itself, etches readily in a Cl$_2$ plasma. However, a native oxide layer covers all aluminum films. Pure Cl$_2$ does not etch this oxide, so BCl$_3$ is added to increase the amount of sputtering and to scavenge the oxygen in the aluminum oxide layer. In most modern integrated circuits the aluminum is alloyed with small amounts (0.5% to 2%) of silicon and copper. Copper in particular is difficult to etch by RIE, so BCl$_3$ is also useful for increasing the amount of physical sputtering which removes the copper. Typically the aluminum itself is removed very rapidly, but complete removal of other metal residue requires a longer etch. A variety of wet chemical etchants can also be used to remove the metallization, but the chemicals will enter the vias and isotropically undercut the next lower metal line.

It is important that aluminum etching be done in a separate reactor (or one that has been cleaned thoroughly) than the reactor used for silicon compound etching. The reason for this is that the chemistries “poison” each other. Fluorine containing polymer residues from oxide etching will react with aluminum to form aluminum fluoride on the metal surface, which is inert to chlorine etch. Aluminum chloride by-products, left behind from the aluminum etch, form an aluminum fluoride powder when exposed to fluorinated plasma: this powder subsequently falls and contaminates the sample surface. Another, important consideration in aluminum etching is moisture contamination. For this reason, as well as safety considerations, a vacuum load-lock is highly recommended for this application.

Obviously, aluminum etching is one of the most difficult processes. However, if done correctly very good etch results can be obtained. A good starting recipe for a more uniform but isotropic etching of the Al is:
Table V: Aluminum etch recipe.
*Note: Lowering the pressure to 30-mTorr will yield an anisotropic etch of the Al, if that is what’s desired.

Polysilicon
Polysilicon can be etched anisotropically & isotropically in chlorine gas, and it is also very selective to oxide. The table below outlines an isotropic & anisotropic etch recipe using Chlorine chemistry:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td>Isotropic: 180-mTorr</td>
<td>Low power = high selectivity = low voltage</td>
</tr>
<tr>
<td></td>
<td>Anisotropic: 30-mTorr</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>100-watts</td>
<td></td>
</tr>
<tr>
<td>Flow</td>
<td>Isotropic: 5-sccm Cl₂</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Anisotropic: 300-sccm Cl₂, 25-sccm HBr</td>
<td></td>
</tr>
<tr>
<td>Etch Rate</td>
<td>Isotropic: 0.5-um/min</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Anisotropic: 0.3um/min</td>
<td></td>
</tr>
</tbody>
</table>

Table VI: Polysilicon etch recipe.

Anisotropic Dielectric Removal vs. Sequential Removal

Anisotropic dielectric removal is useful, but in many situations defects or other features of interest may lie underneath conductors. In this case, metal and dielectric layers must be removed sequentially. Naively, one would expect that a simple reversal of the etch processes used to fabricate the circuit would delayer it. However, it is important to remember that when reactive ion etching is performed during fabrication there is photoresist on the circuit surface to cover up areas that should not be etched, and each etch step usually terminates on an “etch stop”, i.e. a layer which has a very low etch rate for the etch. During sequential delayering, neither of these things is true.

Proper etch recipe selection is crucial to prevent inadvertent removal of layers not intended to be etched. It is important that lower level metals layers are not exposed when the top level metal is etched, or the lower level metals will be removed prematurely.

Oxide Sidewalls
Because interlayer dielectrics are usually quite planar, in principle it is possible to maintain a planar surface during alternate delayering of metal lines and dielectric layers. However, the top most layer of dielectric, usually referred to as the passivation, is not usually planarized. Because this silicon dioxide or silicon nitride layer is conformal, anisotropic RIE removal tends to leave an “oxide sidewall” around the metal line. The sidewall may also contain the aluminum native oxide and a sidewall polymer created during IC fabrication, both of which are very resistant to plasma etching. The sidewall features are difficult to remove by RIE and tend to simply propagate downward during any anisotropic etch. Some success has been achieved at removing the oxide sidewalks using a dilute solution of buffered HF or PSG etch solutions. Adding a higher O₂ content also would solve or reduce this problem.
Planar Delayering
In order to maintain planarity during sequential delayering of an IC, it is desirable to stop each dielectric etch when a level is reached that is even with the next metal layer to be etched. Thus when the passivation is etched, it should be etched level with the base of the metal line. Since there is no etch stop between the dielectric layers, this process requires a timed etch. The time will have to be determined by trial and error for any given integrated circuit process using several test pieces for process development. Failure to time the etch process properly will result in a metal line that is either sitting on top of an oxide pedestal, or contained within a trough. Once the metal line is removed, this pedestal or trough geometry will be propagated downward during the next oxide etch step because the oxide etch is anisotropic. If delayering is not done in a planar fashion, more and more topography will be created that will propagate downward, leaving a very irregular surface. If the objective is simply to remove all metal and dielectric layers so defects on the polysilicon can be viewed, it is probably easiest to dip the part in dilute HF (hydrofluoric acid). HF will isotropically etch all dielectric materials and will undercut the metal lines, thus removing all conductors except the polysilicon.

RIE Grass
RIE grass is an undesirable artifact of etching which prevents a clean delayering of the integrated circuit and interferes with failure analysis. RIE grass occurs when an etch resistant material accumulates in small patches on the sample surface. These patches cause micro-etch-masking, which results in formation of cones. The basic mechanism of cone formation during plasma etching has been understood since the 1940’s. We have found that micro-etch-masking can be due to a complex interaction of sample materials and plasma conditions. It is important to note that once created, the cones tend to propagate downward during the etch, even if the original mask material has been sputtered off. Therefore analysis of the sputter resistant material must be performed early in the development of the cone structures.

Previous reports have identified the cause of RIE grass as sputter re-deposition of package materials, [2,4,5,6] sputter re-deposition of cathode materials, [6,7] and polymer formation. Proposed solutions to prevent RIE grass included covering all gold on the package, [2,4,5,6,7] reducing the RF power, pre-conditioning the chamber, [8] and adjusting the plasma gases and plasma potential. However, a clear presentation of the fundamental sources and solutions to RIE grass has only been recently presented. These mechanisms have been confirmed by Auger analysis.

RIE grass has three basic causes, each of which results in a different physical appearance. The first type of grass is due to sputter re-deposition of package materials and gold leads. Masking these materials from exposure to the plasma is the only way to eliminate this. The second type of RIE grass is due to chemical attack of exposed aluminum metallization, which results in micro-etch masking by aluminum or aluminum compounds. This can be avoided by eliminating O₂ from the gas supply whenever aluminum lines are exposed. The third type of grass is due to a plasma etch chemistry which results in polymer formation on the sample surface. Reducing the gas pressure, which increases plasma potential and therefore increases sputtering, can eliminate this.

The creation of grass and other plasma effects is strongly dependent on the equipment used. Therefore our results are not necessarily applicable to all RIE systems. It is observed that as an RIE system is “conditioned” over time the etching results will drift somewhat from the results obtained in a brand-new system. This conditioning is presumed to be caused by deposition of etch residue on the walls of the reaction chamber. Consistent cleaning of the reaction chamber will bring the etching results to a steady state condition after a short time of use.

Types of RIE Grass
Sputtered Grass
When packaged parts are delayered, it is common that foreign materials on the package will sputter re-deposit onto the die surface causing micro-etch masking and grass formation. By far the most serious problems are produced by gold which is commonly used in ceramic packages (a) in the die cavity for gold/silicon eutectic die attachment, (b) as a metallurgical coating on the lid seal ring, and (c) as gold bond wires. Examples of grass produced by foreign material re-deposition are shown in figure 7.

Gold is easily sputtered by RIE, and the re-deposition of gold onto an IC surface results in severe grass formation. As measured by scanning Auger microscopy, fluorine was not associated with the patches of re-deposited gold. Furthermore the XPS spectra of the gold 4f peaks at 84 eV and 87 eV did not have any binding energy shifts as expected for a gold compound. Therefore we believe that the gold is re-deposited as pure gold.

In order to achieve clean etching, it is essential that all gold on the package be protected from exposure to the plasma. Furthermore, the surface should be thoroughly cleaned to removed any residue or surface impurities that might cause
Plastic covers can be used to protect the lid seal ring from the plasma, but gold bond wires and gold die attach in the cavity are difficult to cover because of their close proximity to the die. Photosist or carbon dag painted on the bond wires and into the cavity will eliminate the gold grass, however the presence of extra organic material can alter the plasma chemistry and increase problems with a different type of grass, such as polymer grass. Using Kapton tape to cover the gold areas and the packaging material is also another option that usually eliminates re-sputtering of any grass-causing foreign material onto the die’s surface.

**Aluminum Grass**

Like gold, aluminum can also sputter re-deposit onto the dielectric surfaces and cause grass. Unlike gold, aluminum is virtually always present within the chip circuitry itself, therefore it is not possible to mask it from the plasma as with gold. Fortunately, etch recipes are available which minimize re-deposition of the aluminum.

For most CMOS processes, the dielectric layers between the conductors are silicon dioxide, and silicon nitride is used only for the top passivation layer. Although a pure CF$_4$ plasma etches silicon nitride slowly, the addition of O$_2$ will increase the fluorine free radical concentration and increase the etch rate of silicon nitride. [10] Therefore, it is common to use a CF$_4$ + O$_2$ chemistry to remove silicon nitride passivation. However, it has been found that once aluminum metal is exposed, the CF4 plasma will attack aluminum re-depositing the etch by-products onto the dielectric resulting in “aluminum grass,” see figure 8. Over time the aluminum lines will become significantly eroded by this etch process, which is also undesirable. Therefore, once the silicon nitride passivation is removed, we change our etch recipe to pure CF$_4$. The pure CF$_4$ recipe does not attack the aluminum, and when run at a lower pressures produces a clean etch with no aluminum or polymer grass. Since a simple change in chemistry eliminates this type of grass, it is reasonable to assume that the aluminum attack is chemical in nature, not physical as commonly believed. This recipe is also more anisotropic and thus less likely to undercut aluminum lines. Unfortunately, pure CF$_4$ is more likely to cause polymer grass, as discussed in the next section.

Some integrated circuit processes use silicon nitride as an interlayer dielectric. For those ICs it is necessary to use SF$_6$ (sulfur hexafluoride) gas to etch the interlayer dielectric, as exposure of aluminum to CF$_4$ + O$_2$ will cause aluminum erosion. Unfortunately, to maintain anisotropy the SF$_6$ process needs to be run at a much lower operating pressure than CF$_4$ and the turbo pump life is adversely affected by sulfur deposits.

**Polymer Grass**

Under certain plasma conditions, carbon-fluorine polymers can form on an integrated circuit surface. [10] This polymer can micro-etch mask the sample surface and produce RIE grass. Polymer grass commonly has the appearance of a fat cylinder with the axis-oriented normal to the sample surface. The top end of the cylinder is often slightly concave. This type of grass is sometimes referred to as “tube worms”, see figure 9. Under slightly different etching conditions, the polymer grass appears as narrow cylinders.

Scanning Auger microscopy of the polymer grass shows a high concentration of carbon and fluorine on the grass. XPS analysis of this layer shows evidence of chemical bonding between the carbon and fluorine. In addition to the usual carbon 1s peak near 285 eV, there is a second peak shifted to 289 eV. This chemical shift is typical for a carbon atom bonded to a single fluorine atom. [11]

The tendency for polymer grass to form is sensitive to both the chemistry of the plasma and materials on the sample surface. The tendency of plasma to produce a polymer is usually described in terms of the fluorine-to-carbon ratio model, [10] where a low ratio of fluorine to carbon is more likely to result in polymer formation. The addition of O$_2$ to CF$_4$ plasma increases the fluorine atomic concentration in the plasma and tends to reduce polymer formation. Thus polymer grass is not formed by the CF$_4$ + O$_2$ plasma used for etching silicon nitride. Addition of H$_2$ or CHF$_3$ to pure CF$_4$ plasma decreases the fluorine concentration in the plasma by forming HF, and this makes polymer deposition more likely. It has been also observed that other sources of carbon on the IC itself can increase the tendency of polymers to form.
The following factors tend to make polymer grass worse:

a. High chamber pressure with pure CF$_4$, especially if the chamber pressure is above 200 mTorr.
b. Addition of CHF$_3$, which is used to improve silicon dioxide to silicon etch rate selectivity.
c. The presence of carbon containing dielectric layers such as spin-on-glass (SOG) or tetraethyl orthosilicate (TEOS) glass.
d. The presence of photoresist or carbon paint used to cover up gold on packaged parts.

The following factors tend to eliminate polymer grass:

a. Reducing chamber pressure, which increases plasma potential and therefore increases sputtering of the surface and removes the polymer micro-etch masks. Typically the silicon dioxide etch was performed at 70 mTorr, which requires a turbo pumped chamber.
b. Addition of O$_2$ to the CF$_4$ chemistry. However, this has the disadvantage of attacking the aluminum and causing aluminum grass.

Our standard silicon dioxide etch works well for silicon dioxide, TEOS, or SOG. If polymer does begin to form, it is necessary to either reduce the chamber pressure or add small amounts of O$_2$ to the gas mixture.

Hybrid Reactors and Deep Oxide (Skeleton) Etching

Keeping devices active during deprocessing can be a major frustration for reliability engineers. Reactive ion etching (RIE) provides a rapid, controlled and acid-free method for delayering integrated circuits. However, RIE places a working device directly on a powered electrode, and this can produce surface contamination, charge damage, and waste many man-hours by destroying one-of-a-kind parts. New HYBRID reactor types solve these problems. [14]

Hybrid reactors are also invaluable in etching deeper than 3 levels of metal. RIE tends to erode the exposed Aluminum as the etch progresses; Hybrid reactors on the other hand are much more delicate in their etching and allows etching which exposed 5 or even 6 levels deep.

Of all the Hybrid reactors, inductively coupled plasma systems are fast becoming the system of choice in front-end production areas. [12,13] They offer many advantages of straight RIE systems such as faster etch rates, cleaner and more selective etches, but also produce much lower plasma damage due to the lower operating voltages or DC bias on the sample surface. These benefits are also important to the failure analysis engineer. Inductively coupled plasma systems or ICP typically contain two RF power sources, one inductive and one capacitive. Each of these power sources introduces energy into the system in different ways. The ICP source introduces energy by the use of an RF induction coil upstream from the sample. The ICP source helps produce a high-density plasma in which there are more free radicals and ions available for reaction. Since most plasma etching is highly dependent on chemical reactions between the gas and the sample surface, the ICP helps produce a higher etch rate. This allows the FA engineer to run a lower RIE power, which is still needed to form a plasma potential at the sample and obtain an anisotropic etch. This way, the inductively coupled plasma system can produce a high etch rate while running at lower RIE power, which produces a lower DC Bias or voltage across the sample. This method achieves two results, fast etching and low device damage.

Deprocessing Results

Figures 10 and 11 show electron micrographs of a three level metal and a four level metal device that were deprocessed down to metal 1. With the ICP, the devices are usually etched more cleanly and with less erosion to the metal lines than the RIE etched devices. Furthermore, with the ICP 4-6 level metal devices can be etched as opposed to the limitations of RIE etching alone. RIE etching alone only accomplishes good etching down to three-level metal. It is important to note that the ICP source does not directly add any power through the sample, it merely enhances the etch rate by increasing the number of reactive species in the reactor. The net effect is the process can be run at lower voltages and maintain a fast anisotropic etch.

Elimination of RIE Grass

All of the mechanisms for RIE grass previously discussed also apply to hybrid reactors. ICP reactors have an added
advantage, because they dramatically increase the operating range of the system. They can be operated at pressures far below those possible in a RIE system (about 1 mTorr). At this pressure no polymer grass can form. Also, they use a lot less power for the RIE bias, and thereby eliminate sputtered grass.

Electrical Damage

The ability to control the voltage at the sample surface is essential to the elimination of charge damage in integrated circuit devices. This is especially important when delayering completed devices to be used for electrical test. The consequence of the reduced voltage in the ICP system should be an improvement in device survival. It is worth mentioning that with lower voltages the heat build up on the sample would be drastically reduced. This also improves the survival of the device during etching. For parts etched down to M1, we found there was no threshold voltage shift for either RIE or ICP etched devices. However, if the polysilicon gates are exposed by deprocessing the damage may be much greater.

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References